Effect of Temperature Cycling and Exposure to Extreme Temperatures on Reliability of Solid Tantalum Capacitors

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I. Introduction

Commercial solid chip tantalum capacitors are typically rated to a temperature range from -55 °C to +125 °C, for both operational and storage conditions. For most electronic components, the storage temperature range is wider than the operational one, and the reason for the relatively narrow storage temperature for tantalum capacitors is not clear. Parts manufactured for the automotive industry, for example THJ capacitors available from AVX, have a continuous operating temperature of 150 °C and are tested by temperature cycling between -55 °C and +150 °C (however, five cycles only).

Military-grade tantalum capacitors manufactured according to MIL-PRF-55365 are rated to the same temperature range as commercial parts. During manufacturing, unmounted parts are subjected to five thermal shocks (TS) between -55 °C and +125 °C as a part of conformance inspection and to 10 TS as a part of qualification inspection (mounted). This means that no testing guarantees that these parts can withstand multiple cycling even within the operating temperature range. Contrary to tantalum capacitors, military-grade ceramic chip capacitors manufactured per MIL-PRF-123 and microcircuits manufactured per MIL-PRF-38535 have much more stringent requirements for temperature cycling (TC). Ceramic capacitors should demonstrate the capability to withstand 100 TS between -55 °C and +125 °C, and the microcircuits during qualification testing are stressed with 100 TC between -65 °C and +150 °C.

MIL-PRF-38534 for hybrid microcircuits requires TC between -65 °C and +150 °C: 10 cycles during screening and 100 cycles during qualification testing. This means that military-grade tantalum capacitors cannot be used in space-qualified hybrids, and DC-DC converters in particular, without additional testing. Note that the same is true for ceramic capacitors, which are tested between -55 °C and +125 °C only. However, contrary to ceramic capacitors, where mechanical stresses are changing substantially after soldering onto a board, in tantalum capacitors, due to the presence of molding compound and metal frame, which might provide some stress relief, the stresses developed during TC are probably similar for loose and soldered parts. This makes TC testing of loose tantalum capacitors more effective and important compared to the ceramic parts.

A recent history of failures of DC-DC converters used in different space projects [1] indicates a relatively large proportion of cases (eight out of 31 reported) where capacitors were the culprits. Similar information was obtained from manufacturers of DC-DC converters, which indicated that failures of tantalum capacitors are the major reason for failures in DC-DC converters during testing. In our experiments, where 10 DC-DC converters were subjected to multiple TC between -65 °C and +150 °C, one part ceased functioning due to a failed/burnt tantalum capacitor. These data suggest the necessity of a more thorough understanding of the robustness of tantalum chip capacitors and their mechanical and electrical integrity after stresses by multiple TC in a wide range of temperatures.

Soldering reflow is one of the most stressful processes for all surface mount technology (SMT) components, and for solid chip tantalum capacitors in particular. Due to mismatch of the coefficients of thermal expansion (CTE) between the constituent materials (molding compound, tantalum, manganese, silver epoxy, and metal frame), significant mechanical stresses develop in the bulk of materials and at the interfaces. These stresses might cause cracking in the tantalum pentoxide dielectric and/or delaminations at the interfaces, resulting in different failure modes of the parts. The cracking increases leakage currents, decreases breakdown voltages, and might cause short-circuit and catastrophic failures in the system. On the other hand, delaminations would raise the effective series resistance (ESR), thus increasing power dissipation and temperature of the capacitor and thereby decreasing its reliability. Severe delaminations might result in intermittent contacts and open-circuit failures of the parts.

Available literature data indicate the possibility of inducing damage to the parts during the soldering process. Edson and Fortin [2] showed that immersion of tantalum chip capacitors into molten solder can increase leakage currents from 0.1 μA to ~100 μA. It was also noted that devices manufactured by different vendors showed different sensitivity to the solder dipping test. Marshall and Prymak [3] indicated that solder reflow conditions in some cases might affect the results of the step stress surge current testing (3SCT) and cause surge current failures. To mitigate problems developed during reflow soldering in tantalum capacitors, a special technique called "proofing" is recommended in [4]. It is assumed that proofing, or controlled power-up of the part after assembly, allows activation of the self-healing effects in tantalum capacitors, and thus reduces failures in low-impedance applications.

A rapid increase of temperature during the solder reflow process might result in a phenomenon specific to plastic encapsulated components and well known for commercial microcircuits, the so-called pop-corning effect. This phenomenon is due to the presence of moisture in polymer materials. When moisture absorbed within the bulk of material or trapped at the interface between molding compound and assembly is rapidly vaporized at high temperatures, a substantial vapor pressure and mechanical stresses develop. In tantalum capacitors, these stresses might be sufficient for causing damage to a thin tantalum pentoxide layer or fracturing the package. This phenomenon was thoroughly studied and is now well contained for plastic encapsulated microcircuits (PEMs). However, the possibility of this effect for chip tantalum capacitors has not been investigated yet.

In this work, results of multiple TC testing (up to 1,000 cycles) of different types of solid tantalum capacitors are analyzed and reported. Deformation of chip tantalum capacitors during temperature variations simulating reflow soldering conditions was measured to evaluate the possibility of the pop-corning effect in the parts. To simulate the effect of short-time exposures to solder reflow temperatures on the reliability of tantalum capacitors, several part types were subjected to multiple cycles (up to 100) between room temperature and 240 °C with periodical measurements of electrical characteristics of the parts. Mechanisms of degradation caused by temperature cycling and exposure to high temperatures, and the requirements of MIL-PRF-55365 for assessment of the resistance of the parts to soldering heat are discussed.

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II. Experiment

Temperature cycling in the range from -65 °C to +150 °C was carried out on six groups of commercial chip and leaded tantalum capacitors and in the range from -65 °C to +125 °C on three groups of military-grade devices. Table 1 displays

part types and test conditions used in our experiments. The dwell time at the temperature extremes was 15 min., and the transfer time was 10 min.

Table 1. Description of parts and test conditions.

Part	Qty.	TC Range, °C	C Limit, %	ESR Limit, Ohm	DCL Limit, μA	Case
2.2 μF/35 V	10	-65 to +150	±10	8	0.8	6032
15 μF/50 V Gr. I	10	-65 to +150	±20	0.3	7.5	7343
15 μF/50 V Gr. II	10	-65 to +150	±20	0.3	7.5	7343
22 μF/35 V	60	-65 to +150	±20	0.7	7.7	7343
10 μF/50 V	10	-65 to +150	±10	1.6	4	leaded
10 μF/25 V	10	-65 to +150	±10	2.5	2	leaded
2.2 μF/10 V	15	-65 to +125	±10	8	1	B
10 μF/25 V	15	-65 to +125	±10	1.4	3	G
22 μF/20 V	15	-65 to +125	±10	0.9	4	H

Note that 10 μF/50 V and 10 μF/25 V were leaded plastic encapsulated devices, whereas all other parts were chip molded tantalum capacitors. Commercial parts were stressed to 500 cycles and military-grade parts to 1,000 cycles with interim measurements of C, ESR, and DCL. The leakage currents were measured at rated voltages while monitoring I(t) characteristics of the parts for 5 minutes and taking the last reading, so DCL = I(5).

Leakage current is the most sensitive indicator of the quality of dielectric in a capacitor compared to the other specified parameters such as C, DF, and ESR. However, DCL has also the largest margin (~ 2 orders of magnitude) between the real values and the specified limits. For this reason, in our experiments the part was considered as a failure when DCL increased more than three times compared to initial value.

Monitoring of the I(t) characteristics was also used to detect scintillation events in the parts. These events are momentary breakdowns in the tantalum pentoxide, and their observation can be used to characterize quality of the dielectric [5]. Typically, in tantalum capacitors current relaxation after application of forward voltage is due to absorption currents and follows a power law: $I \sim t^{-n}$, where the exponent n is in the range from 0.8 to 1.1 [6]. On the I(t) curves, the scintillations appear as short-duration current spikes, which makes this technique a simple and reliable means for detection of the scintillation events.

The probability of surge current failures was estimated by measurements of the voltage, at which a failure during the step stress surge current testing (3SCT) occurs. During this test, the voltage was increased from the rated voltage in 2 V increments until the part failed. The testing was carried out using a PC-based data-capturing system with a field-effect transistor (FET) switch described in [7]. The current transients were monitored using an oscilloscope, and the failure event was determined when the current after the initial spike increased to more than 10 mA.

Temperature dependencies of deformation of chip tantalum capacitors and epoxy molding compounds were measured using a thermal mechanical analyzer, TMA2940, manufactured by TA Instruments. Characteristics of molding compounds, including the glass transition temperature (Tg) and coefficients of thermal expansions, were measured on small pieces of the devices cut from the packages. These measurements were carried out at a rate of 3 °C/min. during cooling from 220 °C, followed by heating of the sample in the analyzer at the same rate. This allowed for monitoring of the stress relief in the sample and assured elimination of possible errors related to the presence of moisture and built-in mechanical stresses. Measurements of deformations of the packages were carried out directly on the parts with a probe placed on the back surface of the plastic case. During these measurements, the heating rate was varied from 3 °C/min. to 20 °C/min. to simulate soldering reflow conditions.

Multiple cycling to high (240 °C) temperatures (HT cycling) was carried out at a heating rate of 20 °C/min. using the TMA chamber. The duration of exposure to high temperatures, 239 °C < T < 241 °C, was ~60 seconds. Four groups of capacitors described in Table 2 were used in this study. Each group had 12 to 15 parts and was subjected to 30 cycles (one group was subjected to 100 cycles) with interim measurements after 1, 3, 10, and 30 cycles.

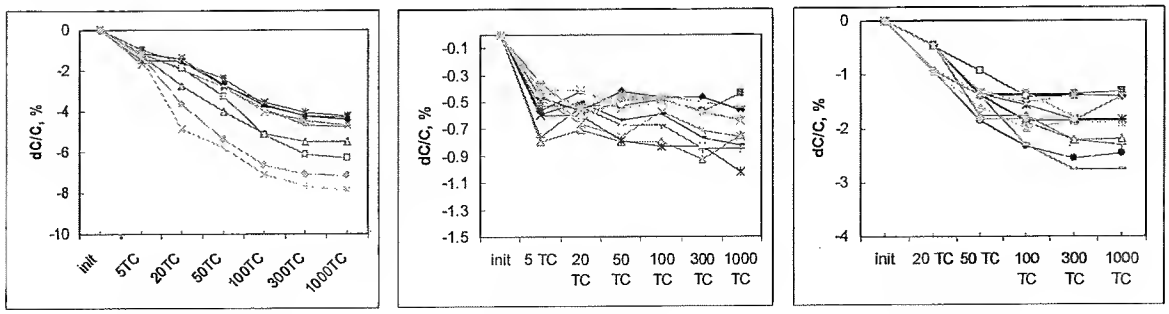
Table 2. Tantalum capacitors used for HT cycling.

Part	C Limit, %	ESR Limit, Ohm	DCL Limit, μA	Case
15 μF/50 V	± 20	0.3	7.5	7343
22 μF/35 V	± 20	0.7	7.7	7343
4.7 μF/50 V	±10	1.5	3	H
22 μF/ 20 V	± 10	0.9	4	H

III. Results of temperature cycling in the military range of temperatures

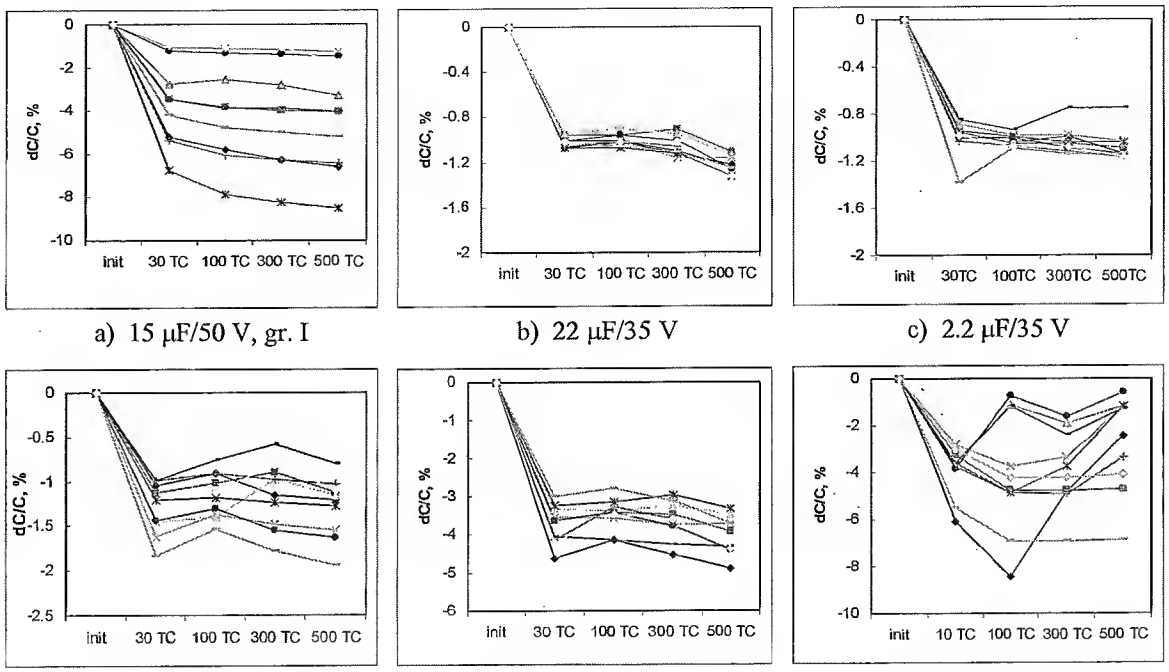
III. 1. Effect of TC on capacitance.

Variations of capacitance during temperature cycle testing for all tested lots are shown in Figures 1 and 2. In all cases, capacitance decreased during the first 10 to 100 cycles and then continued decreasing slowly or stabilized (except for 15 μF/50 V gr. II).



a) 10 μF/25 V b) 2.2 μF/10 V c) 22 μF/20 V

Figure 1. Variation of capacitance in military-grade parts during temperature cycling in the range from -65 °C to +125 °C.



a) 15 μF/50 V, gr. I b) 22 μF/35 V c) 2.2 μF/35 V

d) 10 μF/25 V e) 10 μF/50 V f) 15 μF/50 V, gr. II

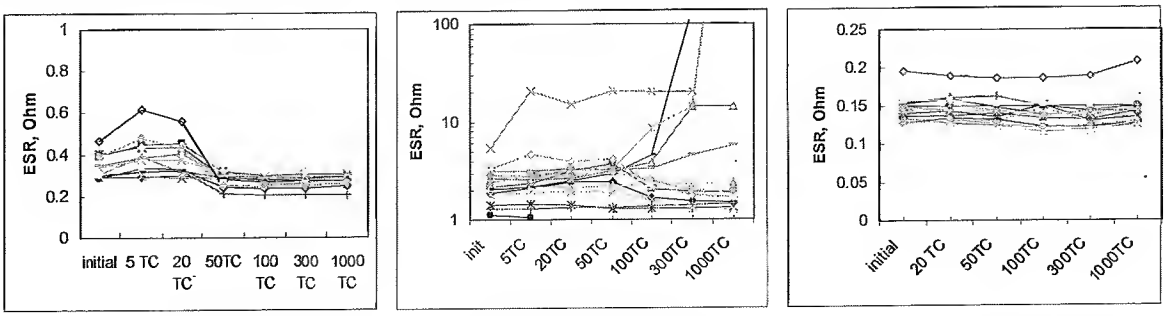
Figure 2. Variation of capacitance in commercial parts during temperature cycling in the range from -65 °C to +150 °C.

The results of cycling between -65 °C and +125 °C show that there is a trend for faster stabilization for smaller-sized capacitors (2.2 μF), where the major drop in C occurs after ~20 cycles. For larger-sized parts, the saturation in C occurs after ~300 cycles. Similar variations in capacitance were observed during cycling of commercial parts up to +150 °C. However, the decrease in C occurs relatively quickly and the capacitance stabilizes mostly after ~30 cycles. The level of the decrease of capacitance varies from ~8% for 15 μF/50 V devices to ~0.7% for 2.2 μF/10 V parts. There is no correlation between the nominal value of the part and its decrease during TC. Note that the behavior of two lots of 15 μF/50 V capacitors was different. Both lots had the most substantial changes during the first 10 to 30 cycles. However, in the first lot capacitance stabilized with the number of cycles, whereas in the second group most of the parts increased C after ~100 TC.

III. 2. Effect of TC on ESR.

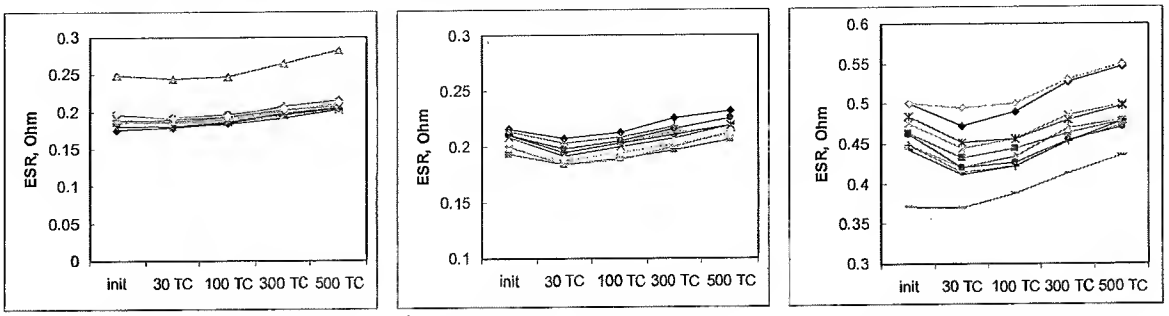
Figures 3 and 4 show variations of ESR with the number of cycles. Two out of three groups of military-grade capacitors, 10 μF/25 V and 22 μF/20 V, did not change the values of ESR significantly. However, the third group, 2.2 μF/10 V, had three failures, and two more parts had a trend of increasing ESR with the number of cycles.

For commercial leaded parts the ESR values did not change significantly with the number of cycles, whereas all chip capacitors manifested some trend of increasing of the ESR after ~30 to 100 cycles between -65 °C to +150 °C. However, this increase did not exceed ~20%, and all ESR values remained well below the specified limits.

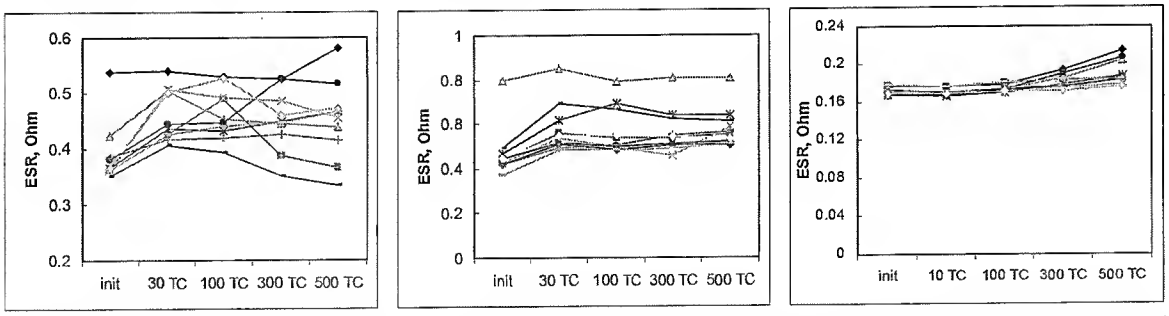


a) 10 μF/25 V, ESR_{max}= 1.4 b) 2.2 μF/10 V, ESR_{max}= 8 c) 22 μF/20 V, ESR_{max}= 0.9

Figure 3. Variation of ESR in military-grade parts during temperature cycling in the range from -65 °C to +125 °C.



a) 15 μF/50 V, gr. I, ESR_{max}= 0.3 b) 22 μF/35 V, ESR_{max}= 0.7 c) 2.2 μF/35 V, ESR_{max}= 4



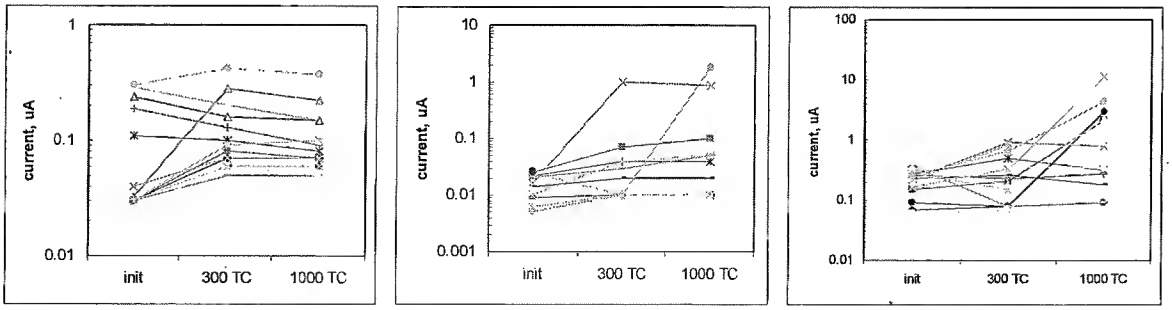
d) 10 μF/25 V, ESR_{max}= 2.5 e) 10 μF/50 V, ESR_{max}= 1.6 f) 15 μF/50 V, gr. II, ESR_{max}= 0.3

Figure 4. Variation of ESR in commercial parts during temperature cycling in the range from -65 °C to +150 °C.

It was assumed that high initial ESR values might indicate potentially defective parts, which have a higher probability of failure during TC. To check this assumption, statistical characteristics of ESR distributions for the 2.2 μF/10 V lot, as well as five other lots manufactured by the same vendor (each lot 20 to 80 samples), were analyzed and compared with the specified limits. The results show that although all 2.2 μF capacitors were within the specification limits, they had the greatest variation of ESR, and one sample exceeded the 3σ limit. The sample, which failed after 5 TC, had also the highest initial level of ESR exceeding the 3-sigma level for this group. This reveals that excessive spreading of the ESR values might indicate the presence of potentially defective parts in the lot. Screening of a lot to pick up capacitors with the lowest ESR values might mitigate the risk and provide additional assurance in the quality of attachment and in mechanical robustness of the parts.

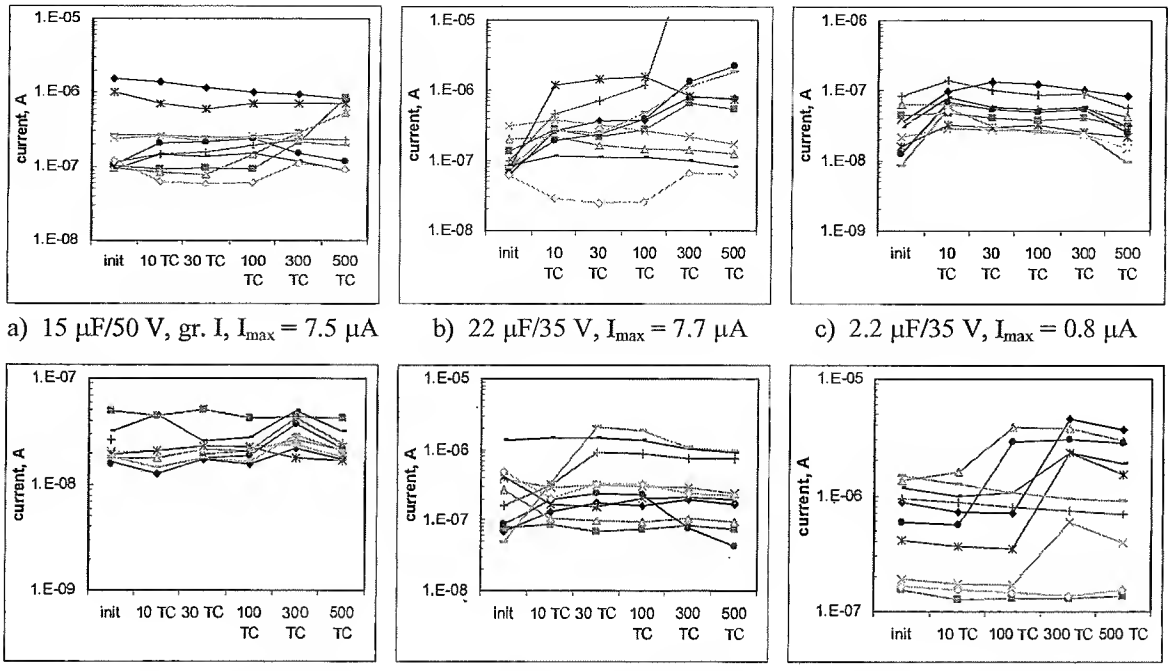
III. 3. Effect of TC on leakage currents

Variations of leakage currents with the number of cycles for all tested parts are shown in Figures 5 and 6. Table 3 summarizes test results by displaying the proportion of parts with substantially increased leakage currents.



a) 10 μF/25 V, I_{max} = 3 μA b) 2.2 μF/10 V, I_{max} = 1 μA c) 22 μF/20 V, I_{max} = 4 μA

Figure 5. Variations of leakage currents in military-grade parts during temperature cycling in the range from -65 °C to +125 °C.



a) 15 μF/50 V, gr. I, I_{max} = 7.5 μA b) 22 μF/35 V, I_{max} = 7.7 μA c) 2.2 μF/35 V, I_{max} = 0.8 μA

d) 10 μF/25 V, I_{max} = 2 μA e) 10 μF/50 V, I_{max} = 4 μA f) 15 μF/50 V, gr. II, I_{max} = 7.5 μA

Figure 6. Variations of leakage currents in commercial parts during temperature cycling in the range from -65 °C to +150 °C.

Table 3. Failures due to increased leakage currents.

TC	2.2 μF/ 35 V	15 μF/ 50 V Gr. I	15 μF/ 50 V Gr. II	22 μF/ 35 V	10 μF/ 50 V	10 μF/ 25 V	2.2 μF/ 10 V	10 μF/ 25 V	22 μF/ 20 V
0	0	0	0	0	0	0	0	0	0
10	0	0	1/10	4/15	1/10	0			
30	0	0	1/10	5/15	2/10	0			
100	0	0	2/10	5/15	2/10	0			
300	0	1/10	3/10	6/10	2/10	0	1/15	1/15	0
500	0	1/10	3/10	6/10	2/10	0			
1000	-	-	-	-	-	-	2/15	1/15	4/15

The results show that only two lots, 2.2 μF/35 V and 10 μF/25 V, had no substantial variation of leakage currents during the testing, while all other lots had 10% to 60% of parts with increased currents. Note that in most cases the currents remained below the specified limits (except for two parts in the 22 μF/20 V group, one part in the 2.2 μF/10 V group, and one part in the 22 μF/35 V group) even after 500 and 1,000 cycles.

III. 4. Effect of TC on breakdown voltages

Typical examples of scintillation events observed during I(t) measurements are shown in Figure 7a, where characteristics of the 22 μF/35 V parts tested after 300 temperature cycles are displayed. During these measurements, most of the parts had a relatively smooth decrease of the current after voltage application, and their I(t) characteristics follow the power law, $I \sim t^{-n}$, where $0.75 < n < 0.95$. However, some parts exhibited current spikes due to a short breakdown in the tantalum pentoxide caused by activation of some flaws in the dielectric. Note that all parts, with and without scintillations, have leakage currents below the specified limits, indicating that the compliance with the specified limits of DCL is not sufficient to assure high quality of the parts.

There was a certain correlation between scintillations and DCL; the parts exhibiting scintillations had larger values of DCL. This means that the parts having excessive leakage currents might have greater propensity to scintillations even when they have DCL below the specified limits, and they should not be used for high-reliability applications.

Variations of the proportion of parts with scintillations during TC for different groups of capacitors are shown in Figure 7b. Interestingly, no scintillations were observed in any of the tested parts up to 30 cycles. However, by 500 cycles only two groups, 2.2 μF/35 V and 10 μF/25 V, had no scintillations, whereas the proportion of defective parts in other groups varied from 10% to 50%. There is a clear trend of the probability of scintillations increasing with the number of thermal cycles.

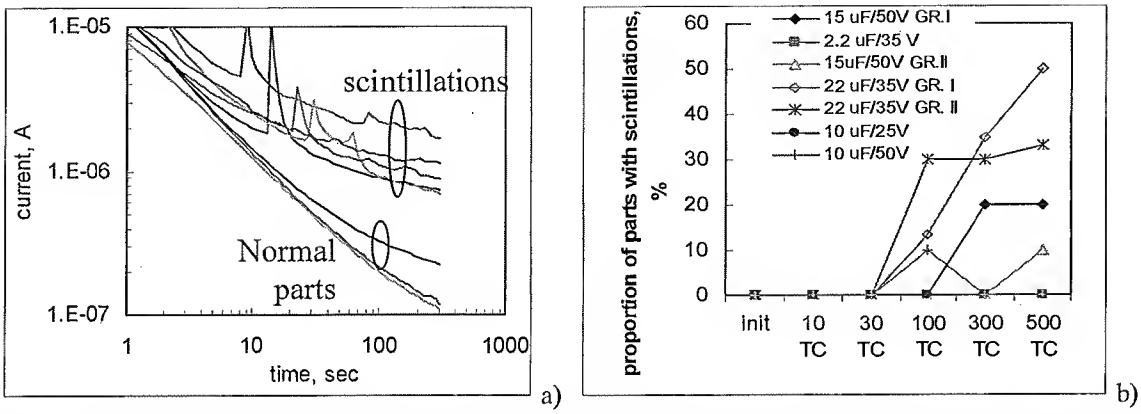


Figure 7. I-t characteristics for the 22 μF/35 V capacitors showing normal parts and parts with scintillations (a) and variation of the proportion of devices with scintillations with the number of TC (b).

Step stress surge current breakdown voltages were measured for 22 μF/35 V capacitors periodically during TC. Due to the destructive nature of this test, a group of 60 samples was used for this testing, and each time during the interim measurements 10 parts were destructively tested and removed from the group. Based on results of these tests, average breakdown voltages, VBR_3SCT, and their standard deviations were calculated. Variations of VBR_3SCT with the

number of cycles are shown in Figure 8a. It is seen that the breakdown voltage gradually decreased during TC testing and varicd from 62.7 V initially to 55.4 V after 500 TC.

Several publications have reported that there is no correlation between the level of leakage current and the probability of surge current stress failures [8, 9]. However, our data (see Figure 8b) accumulated during these experiments indicate that there is a trend of decreasing surge current breakdown voltage for capacitors with greater leakage currents. It is possible, however, that this trend is a result of two different mechanisms occurring during TC, one of which causes an increase in DCL and another one a decrease in VBR_3SCT.

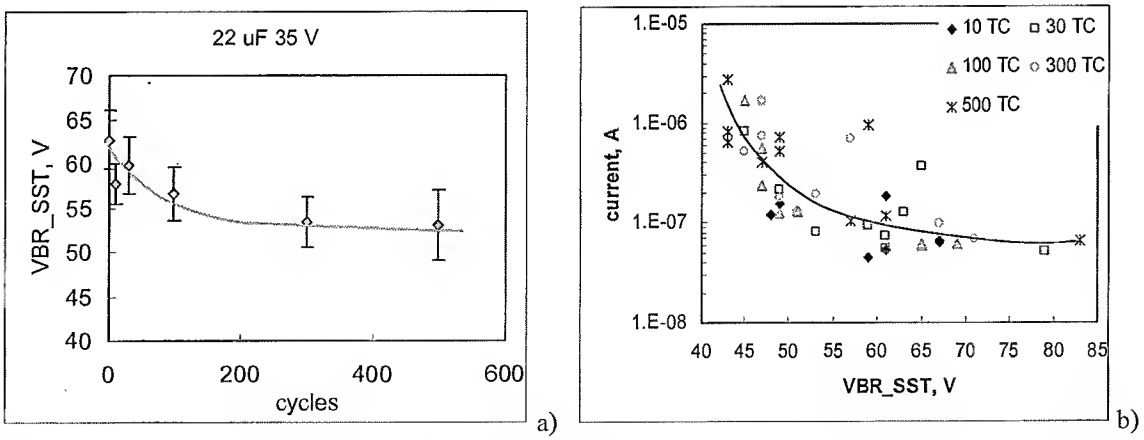


Figure 8. Variation of breakdown voltage during 3SCT with number of cycles (a) and correlation between the VBR_3SCT and leakage current (b).

IV. Discussion of the results of temperature cycling.

1V. 1. Capacitance variations

A decrease in capacitance during TC is due most likely to moisture desorption from the part occurring during the high-temperature periods of cycling. As was shown in our previous work [10], in humid environments moisture condenses in gaps between tantalum pentoxide and manganese cathode, thus increasing the effective area of the electrodes. Typical variations of capacitance caused by moisture sorption at room temperature and ~ 50% RH are in the range from 2% to 10%, and the time for capacitance stabilization during baking at 150 °C is less than 24 hours and at 125 °C is less than 72 hours. Considering that the dwell time at high temperatures during TC is 15 min., this corresponds to less than 100 cycles for 150 °C TC and less than 300 cycles for 125 °C TC. These estimations show that both the value of capacitance decrease and the rate of changes agree with the moisture desorption model.

Variations of capacitance during TC are not related to any degradation process in the tantalum pentoxide dielectric and most likely are not a reliability concern. For this reason, the requirement of MIL-PRF-55365 for capacitance to remain within 5% limits after TS is not justified. More than that, according to the sleeping cells model [10], moisture desorption might be beneficial for reliability of the part. However, a decrease of capacitance during TC for the parts, which had initially the value of capacitance close to the lower limit, would move the part out of specification and formally might be considered as a failure. This failure should be taken into account only if a relatively minor decrease of capacitance would cause malfunction in the system where the part is used, which is not the case for many applications.

It is interesting to note that TC does not affect capacitance of ceramic devices. According to [11], there was no significant difference in capacitance values of ceramic capacitors of various sizes before and after thermal shock. Failures of high-voltage Y5U ceramic capacitors subjected to 300 cycles between -40 °C and +120 °C were due to increased IR, whereas capacitance and dissipation factors remained unchanged [12]. However, multiple cryo-cycling of X5R ceramic capacitors between room temperature and 77 K resulted in 10% to 20% decrease in C [13]. The mechanism of this degradation is not clear.

1V. 2. ESR variations.

Typically, for devices with good cathode attachment, the resistivity of the manganese layer is considered as a major contributor to the ESR of a tantalum capacitor. However, the resistance of interfaces between different conductive

layers of the parts' constitution (manganese, carbon graphite coating, silver paint, silver epoxy, cathode metal) is also critical to assure low ESR values. It was assumed that during TC the mismatch of the coefficient of thermal expansion (CTE) between encapsulating molding compound, metal frame, and silver epoxy would disrupt the interfaces, in particular between the silver epoxy and metal, cause delaminations, increase the resistance of the interface, and thus degrade ESR of the parts.

Out of nine tested lots in our experiments, only one, 2.2 μF/10 V, had ESR failures. Other chip tantalum capacitors manifested only minor (less than 20%) increase in ESR after ~30 cycles. Note that the failed lot was from the same manufacturer that had attachment problems during the period from 1997 to 2000. X-ray images of the part from this lot confirmed poor cathode attachment.

The results suggest that normally, silver epoxy attachment can provide reliable connection of the slug to the cathode terminal, and chip tantalum capacitors are capable of withstanding multiple TC in the military range of temperatures without significant ESR degradation. Non-adequate attachment is a result of poor manufacturing control over the attachment process or materials used, and degradation of ESR during TC might be used as an indicator of these types of deficiencies. Note that measurements of ESR after TS are optional per MIL-PRF-55365. This, as well as a limited number and temperature range of cycling used in the MIL standard, allows potentially defective parts to pass through the screening and qualification process.

IV. 3. Leakage current variations

Considering the sponge-like structure of a tantalum slug; extremely thin dielectric (Ta_2O_5) used; and significant difference in CTE between polymer encapsulant, manganese oxide filling pores in the slug, and tantalum, one might expect that substantial local mechanical stresses would develop inside the slug during TC, resulting in micro-cracking of the dielectric. It is also reasonable to assume that this micro-cracking might cause an increase in leakage currents and failures of the parts.

Three out of nine lots had DCL failures, which exceeded the specified limits, and in seven lots 10% to 60% of the devices manifested a significant increase in leakage currents. In many cases, increased currents did not deteriorate further with increased numbers of cycles. This can be explained assuming that the fatigue-induced cracking ceases to develop as soon as the mechanical stresses are relieved.

Although cracking-induced leakage currents remain relatively low, cracking of the dielectric might facilitate breakdown phenomena and cause scintillations and surge current failures. Note that the two lots, 2.2 μF/35 V and 10 μF/25 V, which had no DCL failures, had also no scintillation failures. This suggests that degradation of leakage currents during TC can be used as an indicator of the quality of the lot.

IV. 4. Breakdown voltage variations

Damage in tantalum pentoxide dielectric, which develops during TC, results not only in increased leakage current, but also increases the probability of scintillation breakdowns. A correlation between the proportion of leakage current failures and portion of parts manifesting scintillations after 500 TC confirms this hypothesis. Similar to leakage currents, in some cases the proportion of parts with scintillations does not increase further with the number of cycles.

Temperature cycling resulted in a relatively small (~12%) decrease in the step stress surge current test voltage. Although this decrease is not substantial, it might result in a rather significant increase in the probability of failures of the parts. Assume that the distribution of VBR_3SCT follows a simple two-parameter Weibull distribution as shown in Figure 9, where the experimental data are approximated with distributions having slopes β ~6.2. In this case, for a part derated to 20 V, the probability of failure due to a surge current event is ~0.06% initially, and it increases more than two times, up to ~0.15%, after 500 TC. It is quite possible that the distribution of VBR_3SCT is two-modal and the low-voltage group of devices has a much larger beta. In this case, the effect of TC on the probability of breakdown would be much more significant. More data are necessary to accurately estimate the VBR-3SCT distribution and its variation caused by temperature cycling.

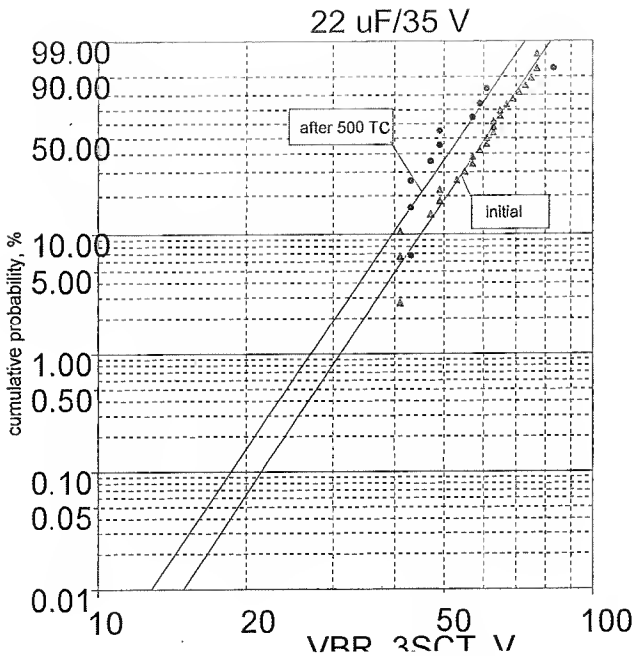


Figure 9. Effect of temperature cycling on distributions of breakdown failures during step stress surge current testing of 22 μF/35 V parts.

Our data indicate an increased probability of failures under surge current conditions after TC for some types of molded chip tantalum capacitors. This is in agreement with the results of R. Franklin [14], who reported that the surge performance of resin-dipped capacitors was also deteriorated by temperature cycling.

V. Thermo-mechanical characteristics of chip tantalum capacitors

Typical results of deformation measurements carried out on 15 μF/50 V capacitors along and across the part at a rate of 3 °C/min. are shown in Figure 10. The TMA characteristics of the molding compound used, which were measured on a piece cut from the part, are also shown on this chart.

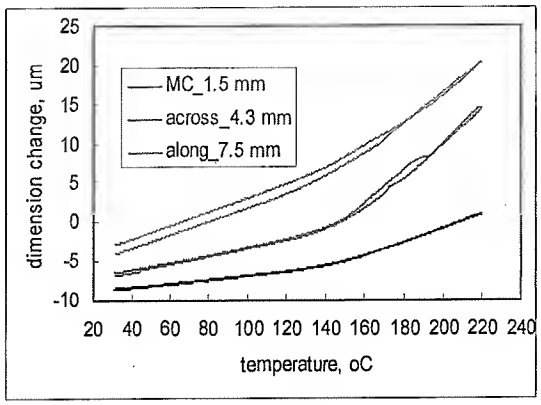


Figure 10. Thermo-mechanical characteristics of a chip tantalum 15 μF/50 V capacitor.

The effective CTE values in glassy (low temperatures) and rubbery (high temperatures) states were calculated as slopes of the curves, whereas a point of inflection of the two straight lines determined the value of Tg. Results of these calculations for 50 μF/50 V capacitors and molding compound (MC) are displayed in Table 4.

Table 4. TMA characteristics of 15 μF/50 V capacitors.

	Tg, °C	CTE1, ppm/°C	CTE2, ppm/°C
Cap. Along	144.2	11.4	26.3
Cap. Across	150.8	11.6	56.4
MC	143.3	17.3	59.2

The results show that the glass transition temperature measured on capacitors and on MC were close and ranged from 144 °C to 151 °C, whereas the effective values of CTE in a glassy state for the part, ~11.5 ppm/°C, were much less than CTE for the MC, 17.3 ppm/°C. A decrease of the effective CTE measured on the part compared to the MC is obviously due to the presence of tantalum slug, which has a CTE = 6.6 ppm/°C and constrains the deformation of the molding compound.

When TMA measurements were carried out on tantalum capacitors at a rate of 20 °C/min., anomalous deformation spikes were detected during the first heating run. Figure 11 shows typical results of these measurements where a spike occurred at ~200 °C, but no anomalies were observed up to 240 °C during the second measurement cycle.

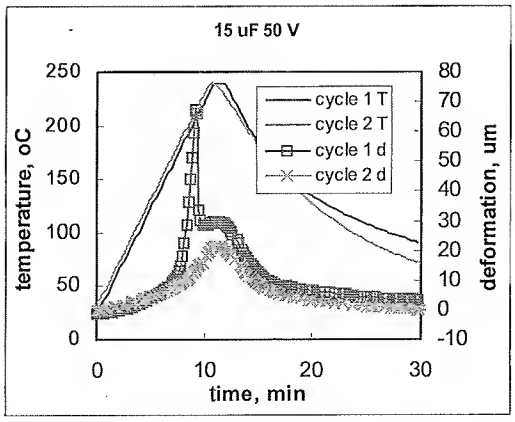


Figure 11. A deformation spike during the first heating cycle on a 15 μF/50 V capacitor. Unmarked lines show temperature variations, and marked lines show deformation of the part.

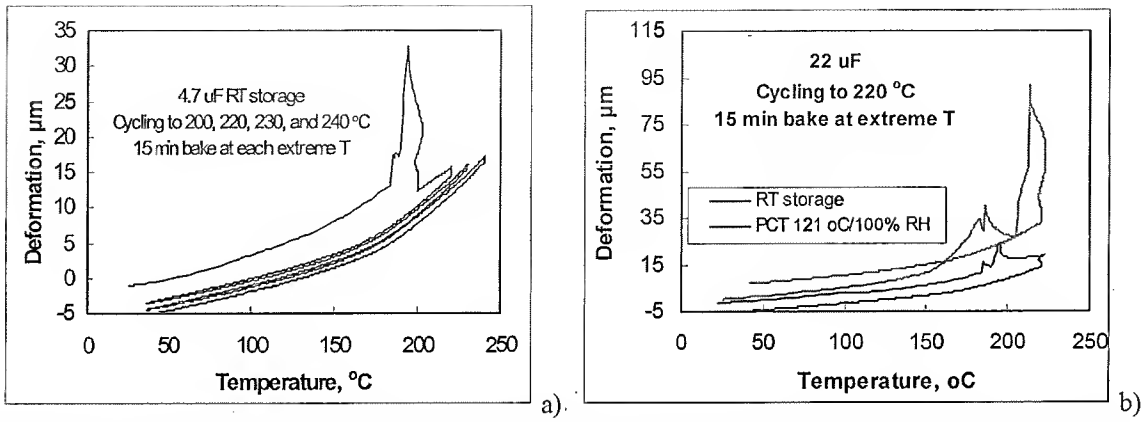
Figure 12a displays results of experiments where 4.7 μF/50 V capacitors were measured at a rate of 20 °C/min., first up to 200 °C, then to 220 °C, 230 °C, and 240 °C. After each temperature extreme, the part was cooled to room temperature. It is seen that the spike appeared during the first temperature cycle only, and cycling to higher temperatures did not cause any anomalies in the deformation.

The effect of moisture preconditioning on deformation spikes was investigated using 22 μF/35 V capacitors. Three groups with three to five samples each were preconditioned at different humid environments: group I was stored in laboratory conditions for 3 months at RH ~40% at room temperature, group II was stored for 1 month in vacuum at room temperature, and group III was moisturized for 96 hours at 121 °C/100% RH (pressure cooker test). Figure 12b shows typical TMA characteristics measured on group I and group III devices having substantial deformation spikes. Parts from the second group did not have substantial spiking.

Results of the tests on all groups are summarized in Table 5 and indicate a clear trend of increasing of the amplitude of spikes after moisture sorption.

Table 5. Amplitudes of deformation spikes, μm, during reflow soldering simulation.

Condition	N	Average	St. Dev.
Long RT	5	17.6	3.7
Vacuum Storage	3	3.8	5.4
121 °C/100% RH	4	47.5	18.6



a) b)

Figure 12. Effect of maximum temperature during HT cycling of 4.7 µF capacitors (a) and effect of moisture preconditioning of 22 µF/35 V capacitors (b) on deformation spikes.

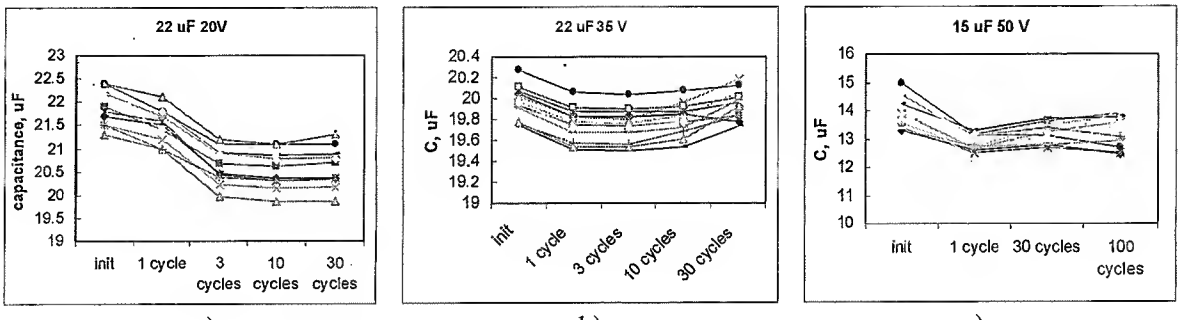
V. 1. Discussion of the pop-corning effect in tantalum capacitors

Deformation spikes during TMA measurements of tantalum capacitors increased with the moisture content of the part and were observed at the first heating cycle and at high heating rates only. The temperature of these spikes was in the range of 180 °C to 200 °C. Similar results were obtained for plastic encapsulated microcircuits. Direct measurements of the deformation during simulated solder reflow on moisturized QFP-132 package style devices revealed deformation spikes up to 200 µm at T ~180 °C [15].

Our results indicate that the pop-corning effect can happen in chip solid tantalum capacitors encapsulated in molding compounds during soldering. However, contrary to plastic encapsulated microcircuits, fractures of the package in tantalum capacitors are relatively rare events. This might be due to a difference in the package design between plastic microcircuits and capacitors allowing relatively large deformations in capacitors to occur without cracking of the package. Nevertheless, excessive deformations of the molding compound in tantalum capacitors during soldering might create substantial mechanical stresses and cause degradation of characteristics or failures in the parts. For this reason, baking of the devices before soldering (e.g., 150 °C for 8 hours) is recommended to reduce the risk of damaging of the parts intended for use in high-reliability applications.

VI. Results of high-temperature cycling

Figure 13 shows variation of capacitance with the number of HT cycles. All parts decreased their capacitance after the first one to three cycles. This decrease varied from 5% to 7% for 22 µF/20 V parts, from 0.9% to 1.3% for 22 µF/35 V parts, and from 2.5% to 12% for 15 µF/50 V capacitors.

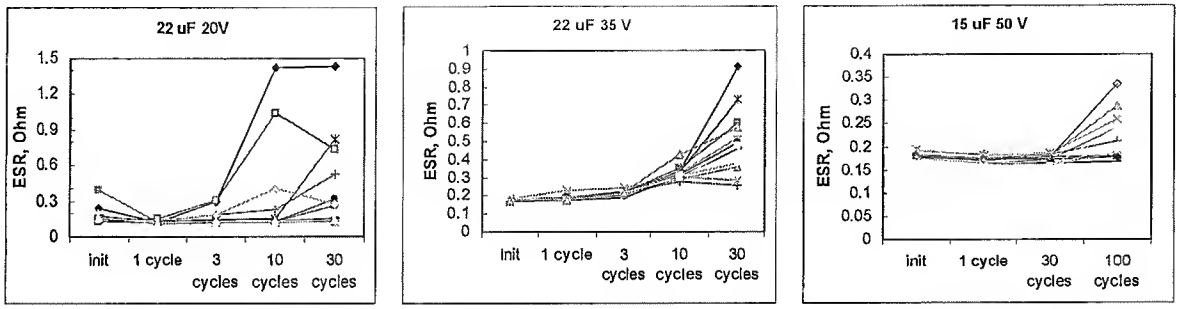


a) b) c)

Figure 13. Effect of high-temperature cycles on capacitance.

The effect of HT cycles on effective series resistance of the parts is shown in Figure 14. In all cases, there is a clear trend of increasing of ESR after 10 to 100 cycles. Two out of 12 22 µF/20 V parts exceeded the specified limit of 0.9 Ohm after 10 cycles, five parts did not change ESR significantly, and the others increased ESR by two to five times after 30 cycles. In the 22 µF/35 V group, one part exceeded the specified limit after 30 cycles, and all others increased ESR values by 1.5 to 5.5 times. All 15 µF/50 V capacitors had stable ESR values after 30 HT cycles, but after 100

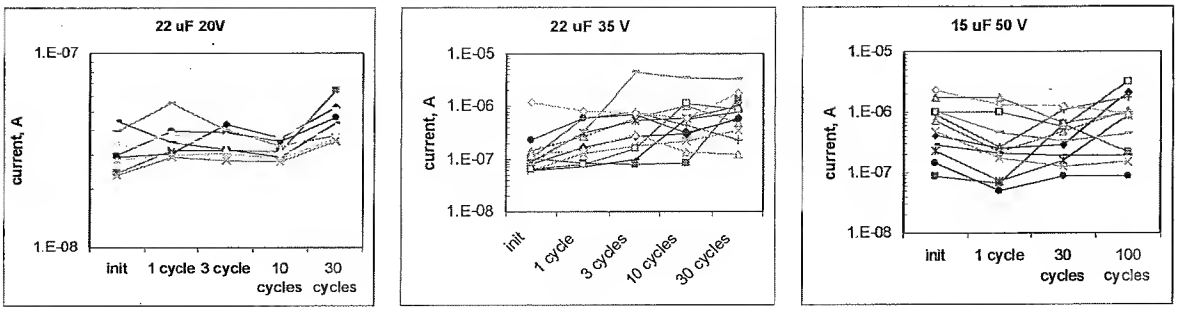
cycles one part failed the specified limit, five parts had no significant variations, and the others increased ESR by 20% to 80% only.



a) limit 0.9 Ω b) limit 0.7 Ω c) limit 0.3 Ω

Figure 14. Effect of high-temperature cycles on ESR. Captions indicate specified ESR limits for the parts.

Variations of the leakage currents during HT cycling are shown in Figure 15. No substantial increase in DCL was observed for 22 µF/20 V parts. Eight out of 12 22 µF/35 V samples increased leakage currents significantly, from three to 40 times. However, these parts did not exceed the specified limit. Only three out of 12 15 µF/50 V capacitors increased DCL by three to five times between 30 and 100 cycles, whereas all other parts had no significant variations.



a) b) c)

Figure 15. Effect of high-temperature cycles on leakage currents.

Results of step stress surge current testing of capacitors before and after HT cycling are summarized in Table 6. The table shows statistical characteristics of the breakdown voltages and results of the analysis based on Student's t-test. At the confidence level of 95%, only 22 µF/35 V parts had significant decrease in the breakdown voltage from 60 V initially to 48 V after 30 HT cycles. Note that as was shown in the previous section of the report, the same lot had a significant decrease in the breakdown voltages after 500 temperature cycles between -65 °C and +150 °C. Variations in VBR_3SCT in other two groups after HT cycling were not significant.

Table 6. Effect of high-temperature cycling on VBR_3SCT.

Part	Initial			After HT Cycling			Analysis		
	Qty.	Avr.	St.	Qty.	Avr.	St.	t	df	$t_{crit, p=0.95}$
22 µF/20 V	10	55.8	9.8	12	53.3	8.9	0.62	18.48	2.10
22 µF/35 V	25	60	10.9	12	48	4.5	4.73	34.56	2.03
15 µF/50 V	8	82.4	11.6	8	90	16.9	-1.05	12.40	2.18

VII. Discussion of the results of HT cycling.

VII. 1. Effect of HT cycling on capacitance.

A decrease in capacitance after one to three HT cycles is most likely related to the same mechanism, which was used to explain the effect of temperature cycling, namely, moisture desorption from the part. Removal of water condensed in micro-voids along the tantalum pentoxide/manganese interface reduces the effective area of the cathode and accordingly decreases capacitance of the part.

Based on temperature dependencies of diffusion characteristics of molding compounds used in tantalum capacitors [10], the diffusion coefficient at 240 °C is D ~5×10^{-6} cm^2/s. Using this value, the characteristic time of moisture diffusion in the package can be estimated as:

$$\tau_D(T) = h^2/D(T),$$

where h is the thickness of molding compound. At h ~0.3 mm τ_D = 180 s. Although this value is greater than the duration of one HT cycle in our experiments (~60 s), a substantial amount of moisture will be desorbed out of the package during first one to three cycles. The duration of HT exposure of the parts during the real soldering process is ~10 s, which might not be sufficient to substantially dry out the part. However, at temperatures significantly exceeding the glass transition temperature of the molding compound, a gap between the tantalum slug and lead frame will be formed, thus substantially enhancing out-diffusion of moisture from the surface of tantalum pentoxide dielectric.

The values of decrease in capacitance caused by HT cycling are in a good agreement with the values of ΔC measured for 22 μF/35 V and 15 μF/50 V capacitors after cycling in the military range of temperatures. However, the results are substantially different (5% to 7% after HT cycling and 1.5% to 2.5% after mil-range cycling) for 22 μF/20 V capacitors. This is due to the fact that the same date code parts were used for cycling of the 22 μF/35 V and 15 μF/50 V capacitors, whereas 22 μF/20 V parts had a different date of manufacturing indicating that moisture-related variations of capacitance are lot related.

Different lots of tantalum capacitors might reduce the value of capacitance due to the moisture removal on 1% to 15% and, similar to temperature cycling, this decrease does not pose any reliability risk to the parts. However, MIL-PRF-55365 requires that the capacitance after resistance to soldering heat test should remain within 5% of its initial value. Note that this is the only parameter that is required to be stable after this test. As our results show, variations of C on more than 5% after soldering simulations are possible and they do not reflect any degradation processes in the part. Failures during this test might be misleading and result in formal rejection of a normal quality lot. Note also that these failures could be easily avoided if the parts are baked before initial measurements and/or are stored for long enough to allow moisture sorption after the testing.

VII. 2. Effect of HT cycling on ESR.

Soldering-related failures due to increased ESR or open circuit are relatively rare but still are known events in the history of applications of tantalum capacitors in high-reliability systems. J. Brusse [16] analyzed failures of military CRW09-style capacitors produced by one manufacturer during the period from 1997 to 2000. Out of 31 failure cases, only six were due to short circuit and 25 to open circuit. Two open-circuit failures were caused by a poor anode wire attachment, but the majority of the parts failed due to the cathode detachment. In most cases, this detachment was triggered by a solder reflow process and is believed to be due to degradation of the silver epoxy/cathode lead frame interface.

In our experiments, ESR values increased after 3 to 30 cycles, suggesting that normally the parts might remain stable after at least three runs during SMT simulation. One of the reasons for the ESR increase after multiple HT exposures might be degradation of the silver epoxy used to attach the tantalum slug to the lead frame. It is known that the contact resistance (Rc) between silver epoxy and non-noble materials, such as Cu, Al, Pb/Sn alloy, etc., increases with time of ageing, especially at high temperatures and humidity. The reason for Rc increase in the presence of moisture is probably due to oxidation of the metal caused by galvanic corrosion at the silver/non-noble metal contacts [17, 18]. Degradation of Rc for Sn/Pb plated metals in dry conditions at temperatures above 150 °C might be caused by the preferential diffusion of Sn from the plating layer into Ag flakes in the conductive adhesive. This diffusion results in formation of Ag/Sn intermetallic compounds in the Ag filler particles adjacent to the plating layer. At high temperatures, micro-voids are created with time in the intermetallics at the Sn/Pb plating layer due to the Kirkendall effect. This process might also result in interfacial de-bonding between the conductive adhesive and the Sn/Pb plating layer [19]. Considering also possible reflow of the tin-based solder during soldering of the capacitors, their use for plating of the lead frames should be avoided for high-reliability parts.

Based on results of capacitance measurements, moisture is mostly released from the part during the first one to three HT cycles. For this reason, the presence of moisture is probably not the major factor of the ESR degradation.

It is possible that the observed degradation is related to fatigue processes caused by thermo-mechanical stresses during HT cycling. Thermo-mechanical stresses in tantalum capacitors might disrupt interfaces at the manganese and/or silver epoxy layers, resulting in increased resistance of the contacts. Additional analysis is required to better understand the reason of ESR degradation after HT cycling.

VII. 3. Effect of HT cycling on leakage current.

The increase of leakage currents during HT cycling in our experiments could be due to either high-temperature degradation of the tantalum pentoxide dielectric or micro-cracking of the dielectric caused by cycling-induced fatigue. It is known that high-temperature annealing of deposited tantalum pentoxide films results in two opposite and competing processes: annealing of the defects and creation of a crystal phase [20]. Crystallization of amorphous Ta_2O_5 films occurs after rapid thermal annealing at relatively high temperatures above 650 °C [21] and results in significant increase of the leakage currents. On the other hand, annealing of the films below the re-crystallization temperature in nitrogen [22] or oxygen [23] environments significantly reduces leakage currents in the oxide by removal of certain structural imperfections present in the layers initially. Oxygen might play an important role in the annealing process by reducing concentration of the oxygen vacancies and/or broken bonds. This decreases the concentration of electron traps in the film and leads to lower leakage current levels.

These results indicate that an increase in DCL after HT cycling observed in two out of three lots in our experiments is most likely due to the cycling fatigue effect rather than to short-term, high-temperature baking of the capacitors. Note also that the lot having the most substantial degradation of ESR (22 µF/20 V capacitors) had stable leakage currents through the testing, which is related to different mechanisms of degradation for ESR and DCL. To assure the resistance of tantalum chip capacitors to soldering conditions, both parameters should be controlled during qualification testing of the parts.

VII. 4. Effect of HT cycling on surge current breakdown.

A significant decrease in the breakdown voltages measured during step stress surge current testing was observed only for one lot, 22 µF/35 V. Interestingly, the same lot had the largest proportion of devices with increased leakage currents, implying a possible correlation between the DCL and breakdown voltages.

Figure 16a shows Weibull distributions of the breakdown voltages measured on the non-stressed 22 µF/35 V devices and those stressed by 30 HT cycles. An increase of the slope of the distribution (β) after HT cycling results formally in a substantial decrease of the probability of surge current failures at voltages below the rated one. This is most likely due to the bimodal character of the distributions, where a group of low-voltage devices has much greater values of β compared to the group of high-voltage devices. The same experimental data as in Figure 16a are approximated with bimodal distributions in Figure 16b. In this case, the probability of surge current failures at voltages below the rated voltage increases more than 10 times after HT cycling. More data are necessary to accurately evaluate distributions of the breakdown voltages and their variations for a low-voltage and high-voltage groups due to exposure to soldering temperatures.

VIII. Analysis of MIL-PRF-55365 requirements.

During screening per MIL-PRF-55365 (conformance inspection), all parts should pass reflow conditioning (one thermal shock to 230 °C minimum with time at T > 230 °C 5 s minimum) to help to remove components with weak internal bonds. However, ESR measurements are optional during the tests following reflow conditioning, so the parts with poor attachment cannot be screened out. Besides, no environmental preconditioning is required. As was shown above, parts exposed to different environments will have different moisture content and might create different level of stress during soldering simulation.

More comprehensive evaluation of the robustness of the parts to soldering stress is expected during a sample-based qualification testing of the lot. Qualification testing per MIL-PRF-55365 evaluates the susceptibility of the parts to solder reflow stress during the resistance to soldering heat (RSH) test. For this test, 18 samples are soldered onto a board at +245 °C ±5 °C and then subjected to a moisture resistance test. Only DCL, capacitance, and dissipation factor are measured before and after the RHS testing, and one out of 18 parts can fail this combined RSH/moisture resistance test. The existing qualification testing has several deficiencies and is not sufficient for assuring adequate reliability of the devices after soldering:

- Only moisture resistance testing is performed following RSH, whereas reliability qualification life test and surge current testing can be carried out without reflow soldering (mounting is optional for life test). Results of reliability testing on as-manufactured parts and parts that have experienced soldering stress might be different. Note, for example, that life testing of PEMs per JESD22-A113 is performed after solder reflow simulation.
- No environmental preconditioning is required before RSH testing. However, due to the pop-corning effect in tantalum capacitors, it is reasonable to expect that the parts with greater moisture content would be more susceptible to formation of soldering-induced defects. Compare this with a system of moisture sensitivity levels

(MSL) developed for PEMs to address this issue and a special procedure including moisture soak, SMT simulation, and flux application used as preconditioning to simulate stresses during soldering.

- Only DCL, DF, and C are required to be measured and remain within the specified limits after resistance to soldering heat test. However, it was shown above that capacitance variations in most cases are not related to degradation processes in the part, and the requirement for capacitance to remain within 5% might be misleading. Also, the real values of leakage currents are typically ~2 orders of magnitude lower that the DCL limits, so even parts with significantly increased leakage currents might be considered as passing the test.
- Only one heat cycle during the resistance to soldering heat test is allowed. Compare this with the requirements for PEMs, where the parts are subjected to three consecutive runs simulating solder reflow process before reliability qualification testing. Our results show that normal quality tantalum capacitors are capable of withstanding three reflow cycles, and this requirement should be used to evaluate their robustness to soldering.
- The effect of soldering reflow on the susceptibility of tantalum capacitors to surge current failures is not assessed. However, our data as well as technical literature indicate that for some lots soldering stress might be significant enough to increase the probability of surge current failures.
- Leakage currents, ESR, and breakdown voltages measured during step stress surge current testing are the most important and sensitive parameters to the reflow soldering stress. Measurements of these parameters, their acceptable variations, and proper preconditioning of the parts before qualification testing should be specified in MIL-PRF-55365 to assure that the reliability of solid chip tantalum capacitors remains high after soldering.

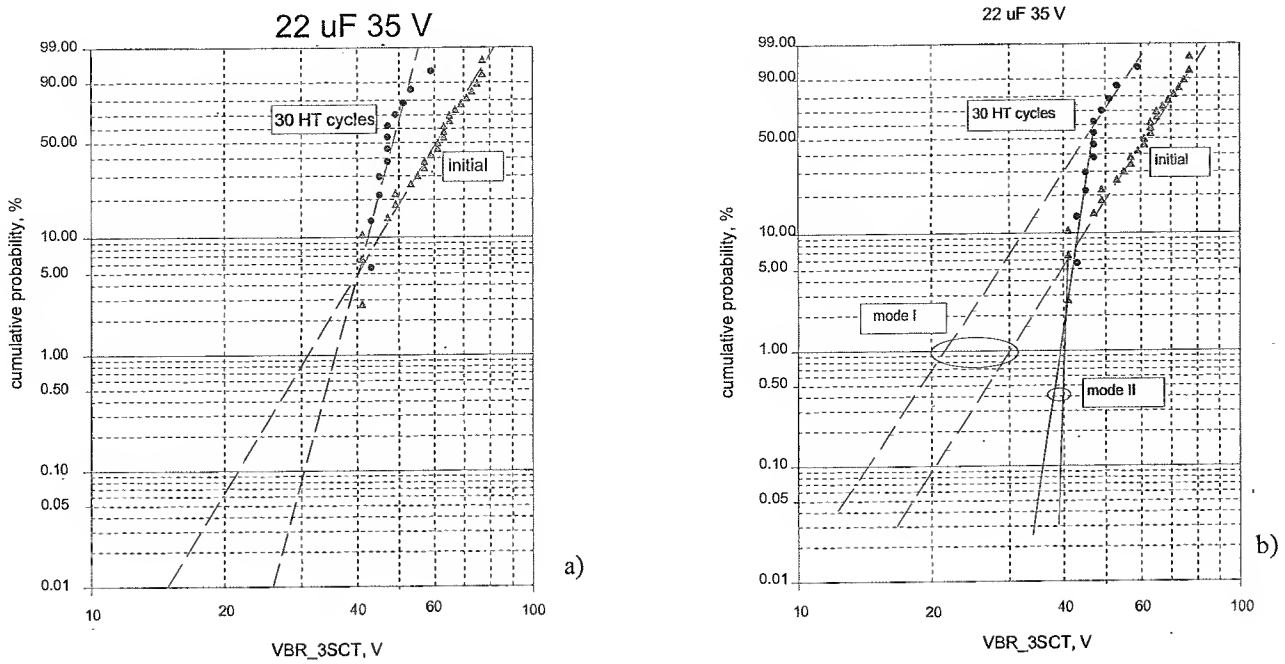


Figure 16. Effect of high-temperature cycling on results of step stress surge current testing of 22 μF/35 V capacitors. The results are approximated with unimodal Weibull distributions in (a) and with bimodal distributions in (b).

IX. Conclusion.

1. Three groups of military-grade capacitors and six groups of commercial tantalum capacitors were subjected to multiple temperature cycling in the range from -65 °C to +125 °C and -65 °C to +150 °C. The results indicate the following:
   a. Tantalum chip capacitors are capable of withstanding up to 500 TC in the temperature range from -65 °C to +150 °C. However, different lots have different robustness under TC conditions and, although the parts might not fail formally by exceeding the specified limits, a significant degradation in leakage current and breakdown voltages indicates an increased propensity of some lots to failure after TC.

b. Temperature cycling up to 150 °C results in decrease in capacitance of 1% to 8%, with most changes occurring after first 10 to 30 cycles. This decrease is most likely due to moisture desorption from the manganese/tantalum pentoxide interface and does not pose a reliability risk.

c. No substantial degradation of ESR was observed in eight out of nine lots even after 1,000 TC. ESR failures in one lot were likely due to poor attachment during manufacturing. This lot had also excessive ESR scattering, which might be used as an indicator of manufacturing deficiencies. Parts with relatively large ESR values, exceeding the 3-sigma limit, might have a higher probability of failure during temperature excursions and should not be used for high-reliability applications.

d. Significantly increased leakage currents after TC were observed in seven out of nine tested lots, and three lots had failures due to exceeding the specified DCL limits. There was no substantial difference in the behavior of commercial and military parts, probably due to the lack of requirements for TC in MIL-PRF-55365.

e. There is a trend of increasing scintillation breakdowns with the number of cycles. No scintillations were observed up to 30 TC, but by 500 TC only two out of nine lots had no scintillations. TC might increase the probability of surge current failures; an average breakdown voltage during step stress surge current testing of 35 V capacitors decreased from 62.7 V initially to 55.4 V after 500 cycles.

f. The requirements of MIL-PRF-55365 regarding TC testing are much less severe compared to ceramic capacitors and microcircuits and are not sufficient to assure the necessary reliability in military-grade hybrids without additional testing. The requirement for ESR measurements after TS during screening should be made mandatory in MIL-PRF-55365, whereas the requirement for capacitance to remain within the 5% limits is not necessary.

g. At least a 100-cycle test within the military range of temperatures should be included in the MIL-PRF-55365 standard, and variations of DCL, ESR, and breakdown voltages should be used to assess the results of this testing. The relevant techniques for breakdown voltage measurements (scintillations and step stress surge current testing) should be specified and used for assessment of the robustness of tantalum chip capacitors.

2. Measurements of deformation of chip tantalum capacitors during soldering simulations showed the presence of anomalous spikes at temperatures from 180 °C to 200 °C, indicating the pop-corning effect. For high-reliability applications, baking of the devices before soldering is recommended to reduce the risk of damaging the parts.

3. Three lots of chip tantalum capacitors were subjected to multiple temperature cycling between room temperature and 240 °C to simulate thermal stresses in the parts during reflow soldering. The results of HT cycling indicate the following:

   a. Exposure to high temperatures might cause degradation of leakage currents and ESR and increase the probability of surge current failures. Different lots have different susceptibility to soldering stress.

   b. After the first one to three high-temperature exposures, the capacitance in all parts decreases by 0.9% to 15%. The effect is most likely due to moisture desorption and is not a reliability concern.

   c. All tested parts withstood three HT cycles without substantial variations of ESR, but additional cycling increases the resistance indicating the onset of wear-out degradation. The number of cycles to this degradation is lot-dependant and varied from 10 to 100 cycles.

   d. A significant increase in leakage current was observed in two out of three lots, and one of these lots had also decreased surge current breakdown voltages.

4. Recommendations to improve screening and qualification testing per MIL-PRF-55365 to assure better resistance of the parts to soldering stress are discussed.

X. Acknowledgement

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